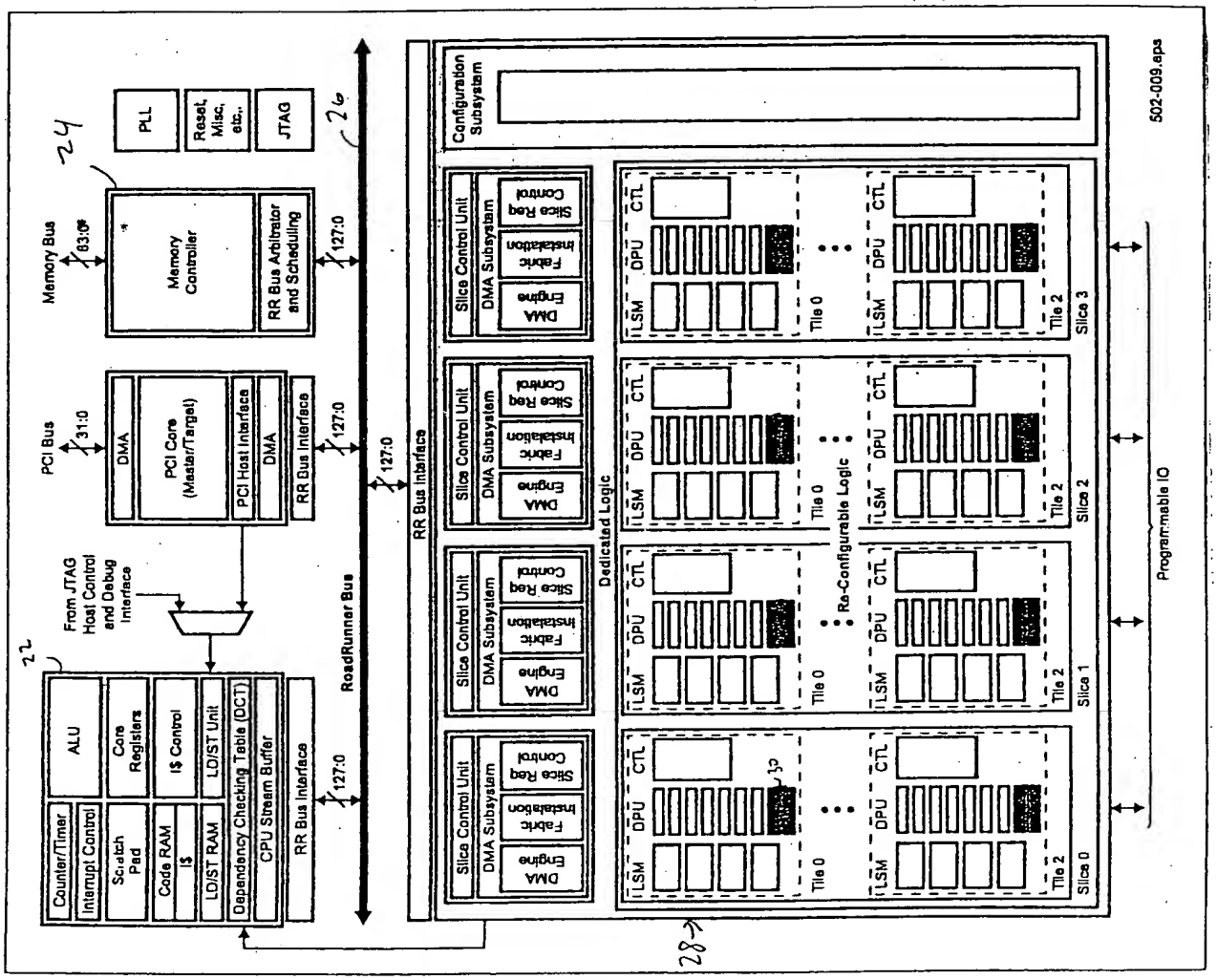

FIG. 1

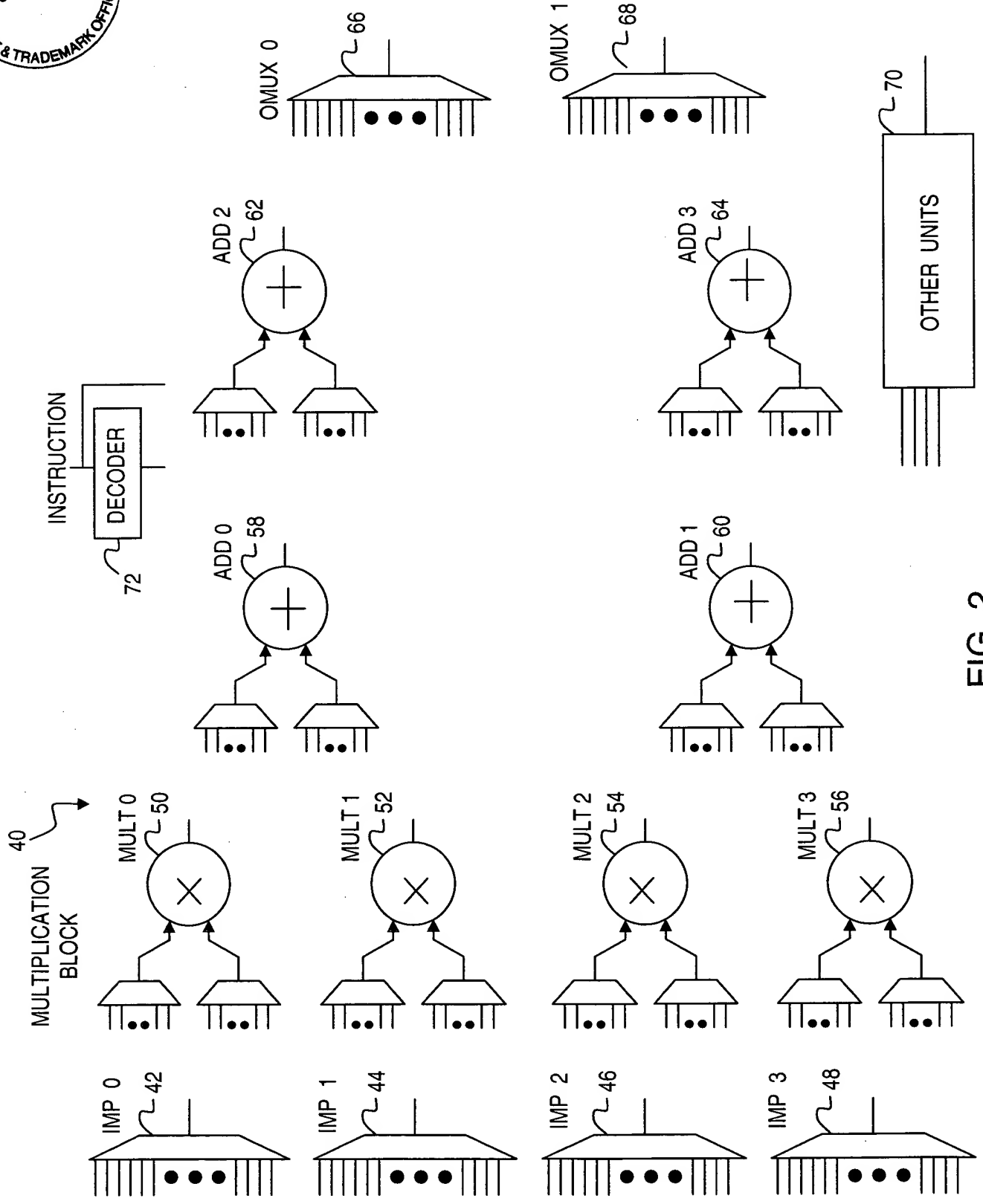

FIG. 2

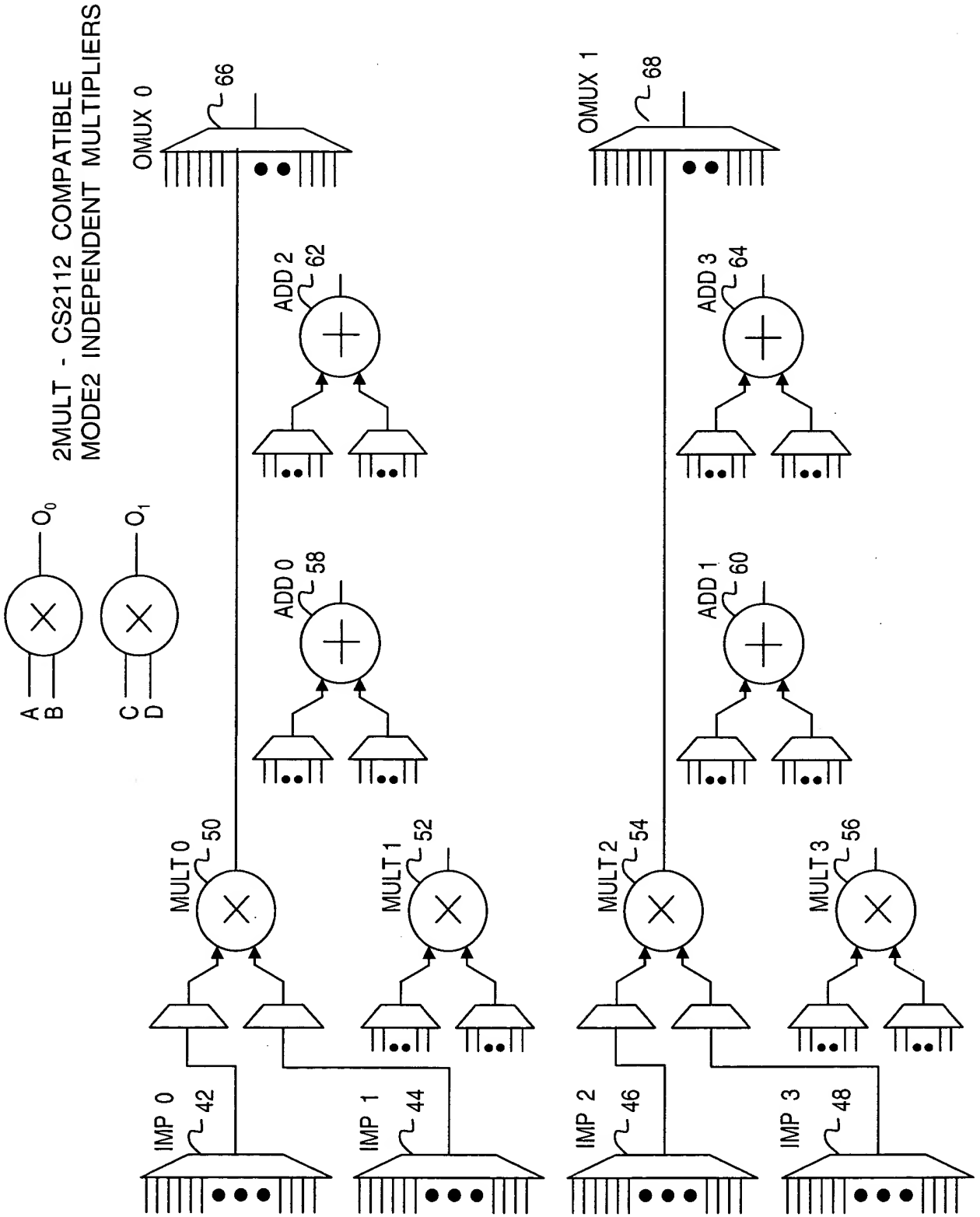
2MULT - CS2112 COMPATIBLE
MODE2 INDEPENDENT MULTIPLIERS
A
B
C
D
O_0
O_1
OMUX 0
66
OMUX 1
68
ADD 2
62
ADD 3
64
ADD 0
58
ADD 1
60
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48

FIG. 3A

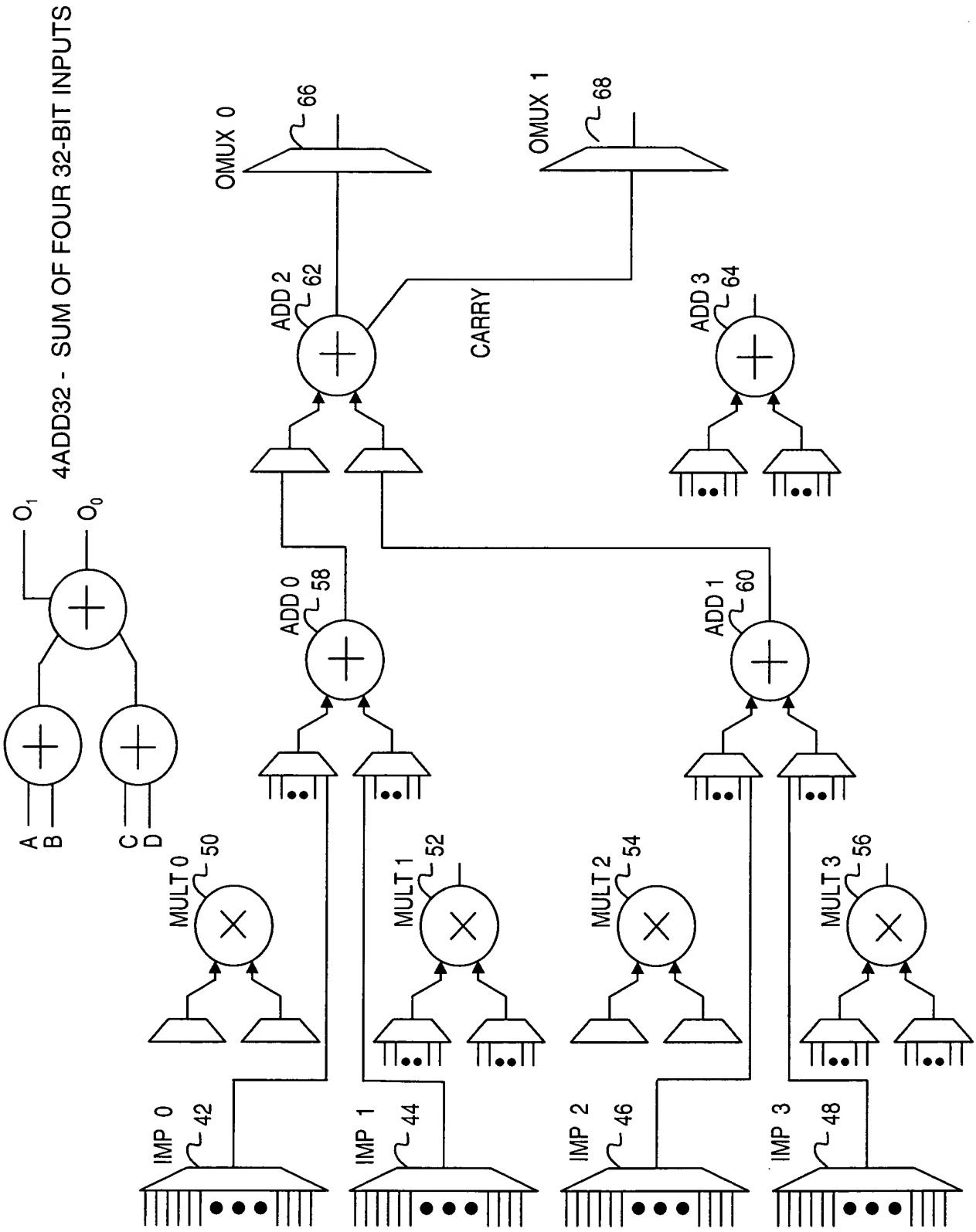
4ADD32 - SUM OF FOUR 32-BIT INPUTS
O_1
O_0
A
B
C
D
OMUX 0
66
OMUX 1
68
ADD 2
62
CARRY
ADD 3
64
ADD 0
58
ADD 1
60
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48

FIG. 3B

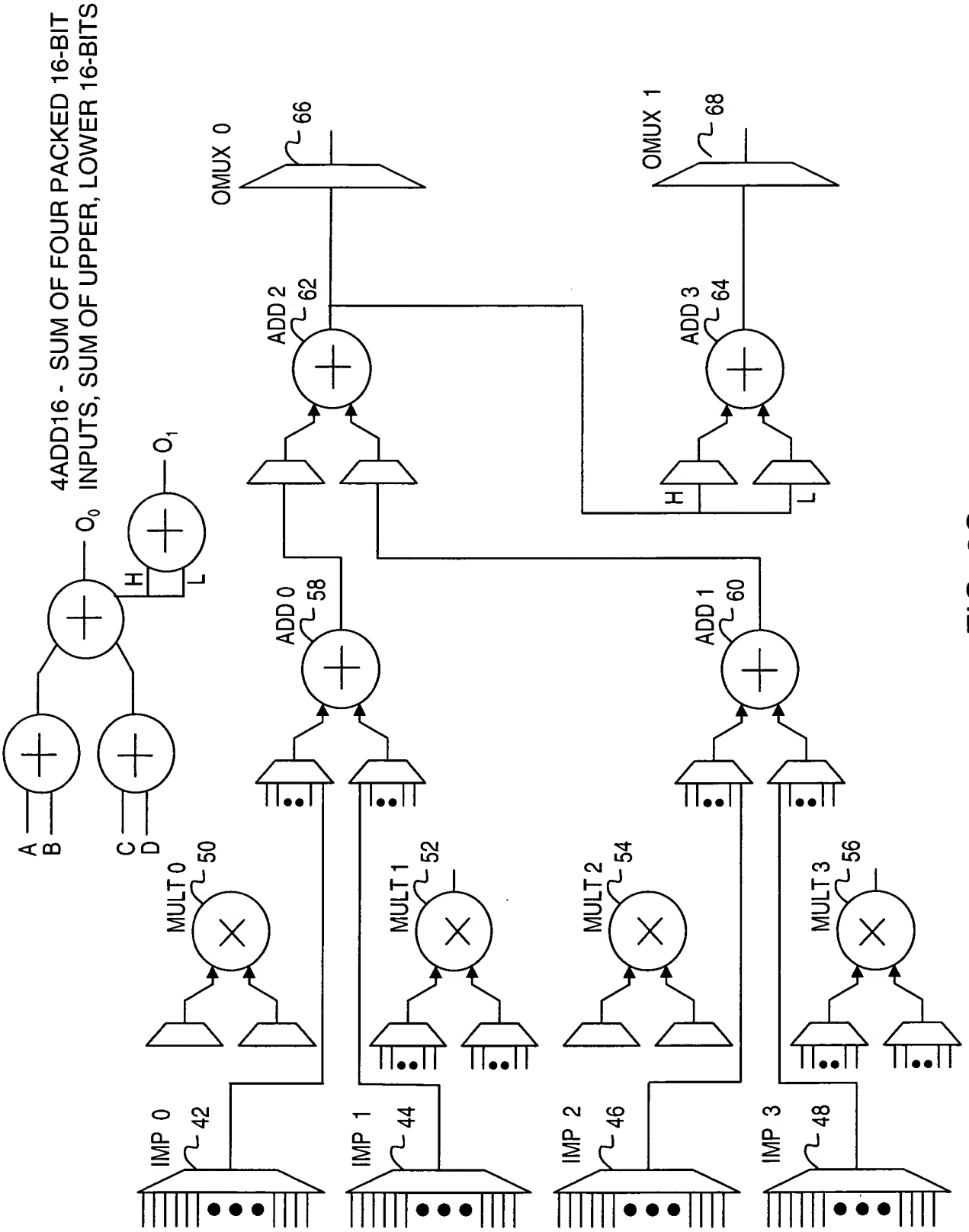
4ADD16 - SUM OF FOUR PACKED 16-BIT INPUTS, SUM OF UPPER, LOWER 16-BITS
A
B
C
D
O_0
O_1
H
L
IMP 0 42
IMP 1 44
IMP 2 46
IMP 3 48
MULT 0 50
MULT 1 52
MULT 2 54
MULT 3 56
ADD 0 58
ADD 1 60
ADD 2 62
ADD 3 64
OMUX 0 66
OMUX 1 68

FIG. 3C

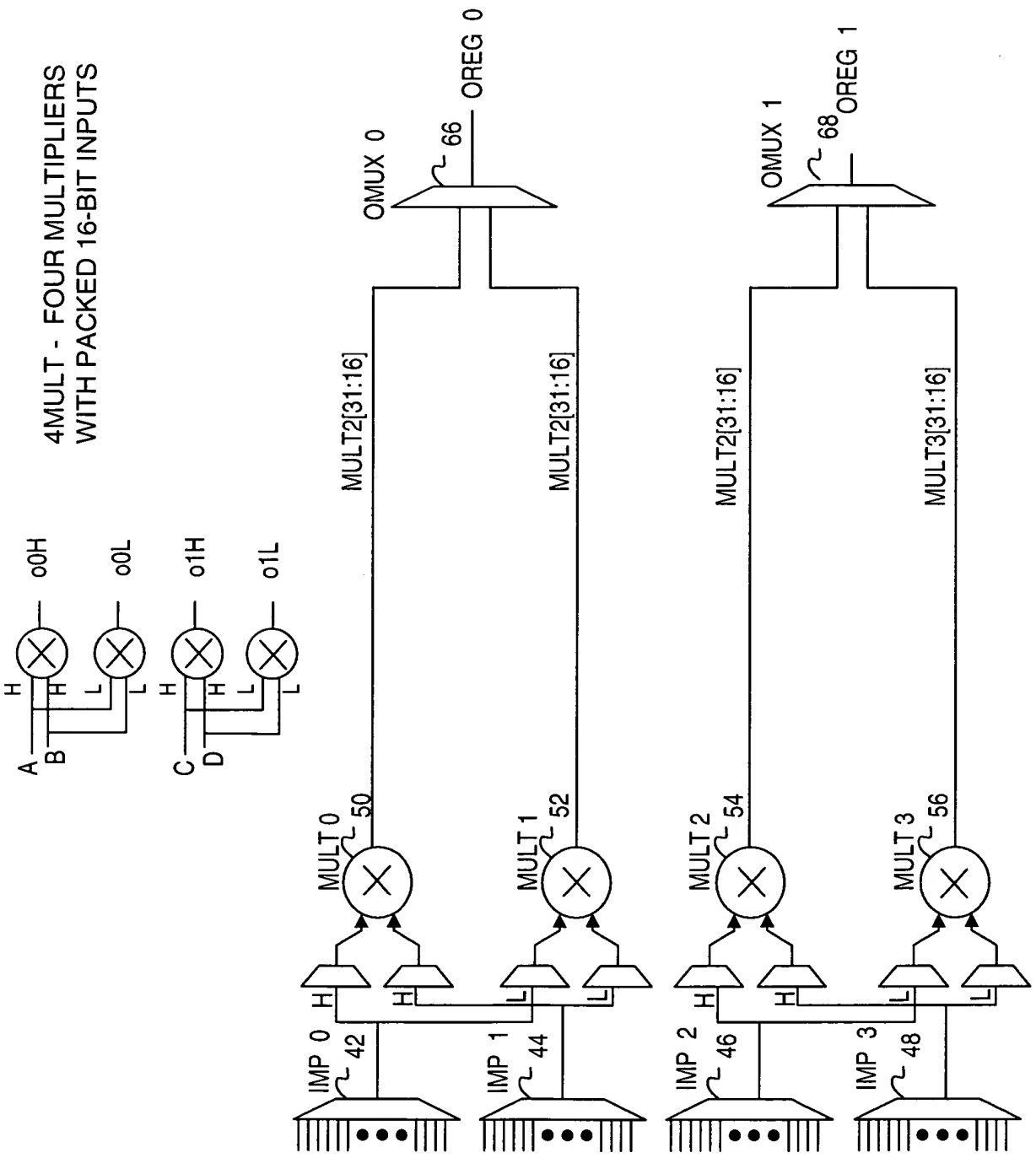
4MULT - FOUR MULTIPLIERS
WITH PACKED 16-BIT INPUTS
A
B
C
D
H
L
o0H
o0L
o1H
o1L
OMUX 0
OREG 0
66
OMUX 1
OREG 1
68
MULT2[31:16]
MULT2[31:16]
MULT2[31:16]
MULT3[31:16]
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48

FIG. 3D

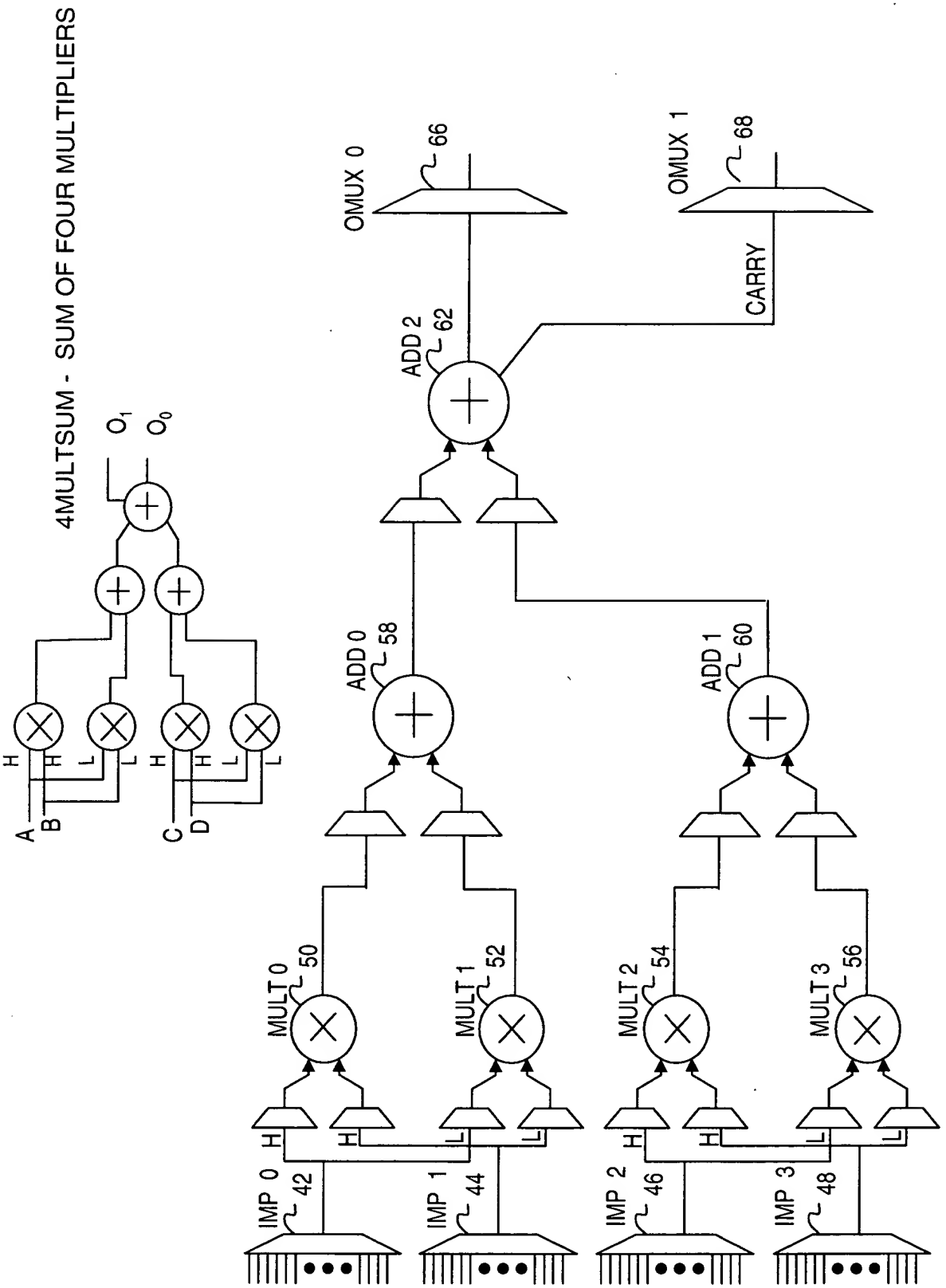
4MULTSUM - SUM OF FOUR MULTIPLIERS
O_1
O_0
A
B
C
D
H
L
OMUX 0
66
OMUX 1
68
CARRY
ADD 2
62
ADD 0
58
ADD 1
60
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48

FIG. 3E

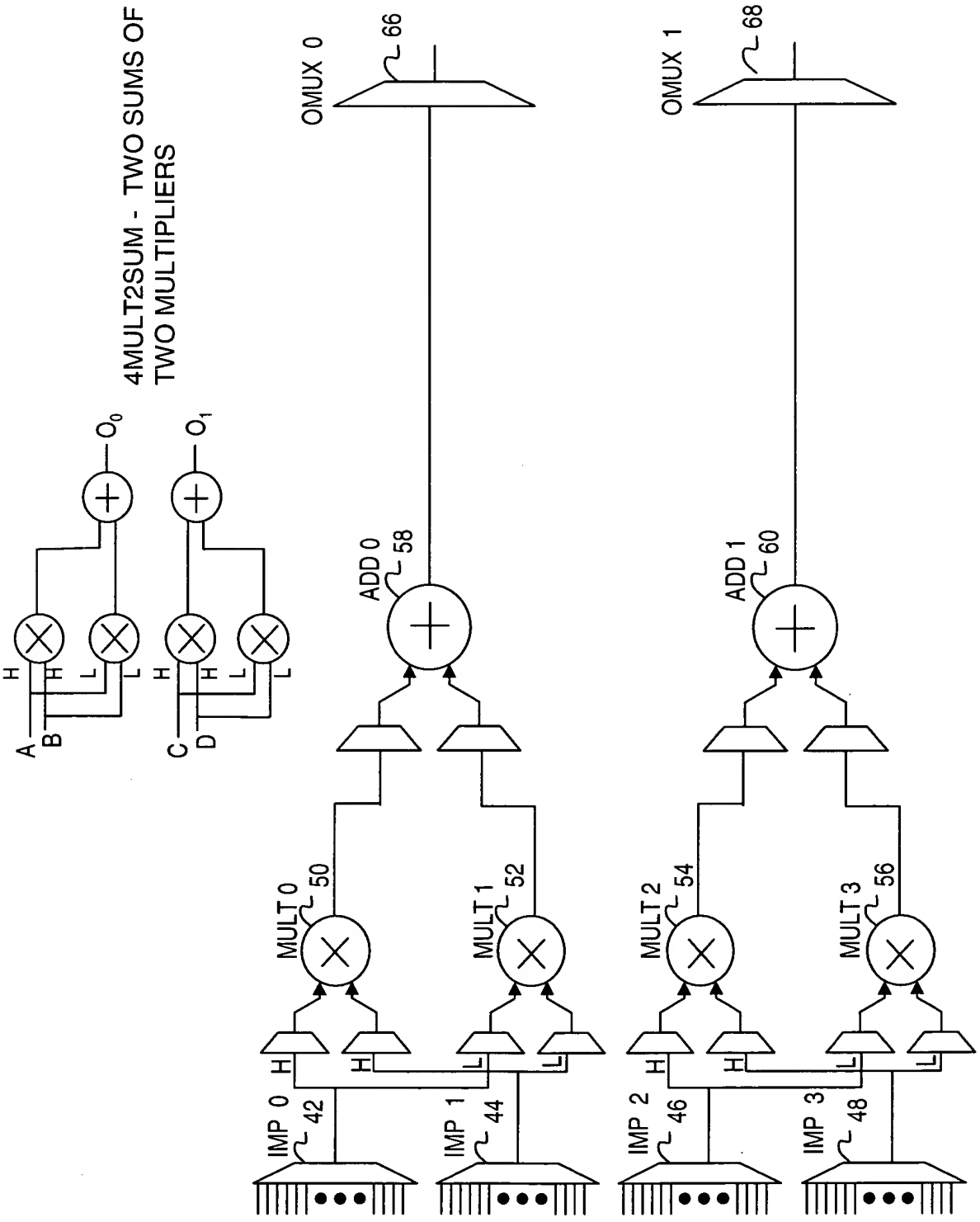
4MULT2SUM - TWO SUMS OF TWO MULTIPLIERS
A
B
C
D
H
L
O_0
O_1
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
ADD 0
58
ADD 1
60
OMUX 0
66
OMUX 1
68

FIG. 3F

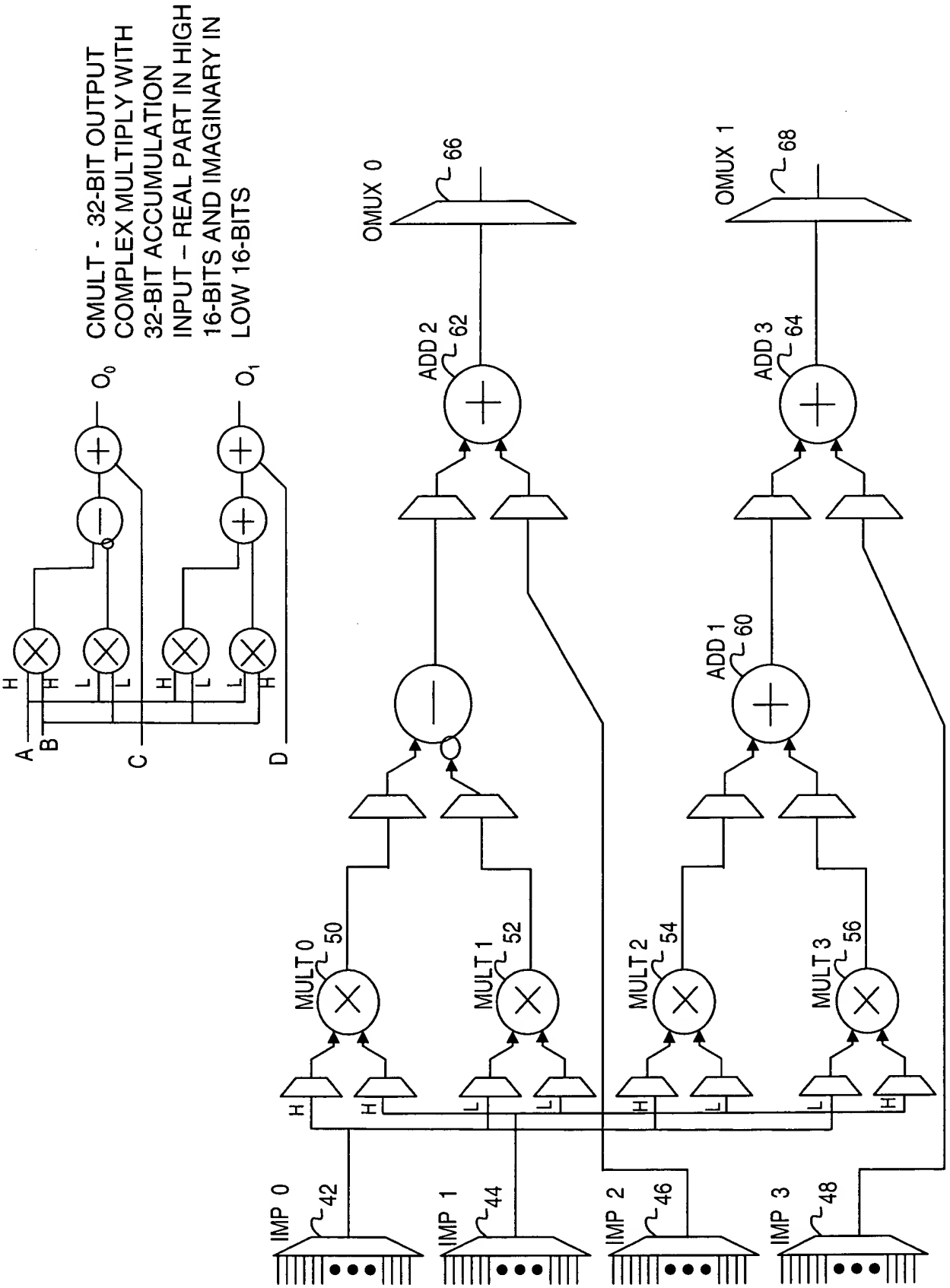
CMULT - 32-BIT OUTPUT
COMPLEX MULTIPLY WITH
32-BIT ACCUMULATION
INPUT – REAL PART IN HIGH
16-BITS AND IMAGINARY IN
LOW 16-BITS
O_0
O_1
A
B
C
D
H
L
IMP 0
IMP 1
IMP 2
IMP 3
42
44
46
48
MULT 0
MULT 1
MULT 2
MULT 3
50
52
54
56
ADD 1
ADD 2
ADD 3
60
62
64
OMUX 0
OMUX 1
66
68

FIG. 3G

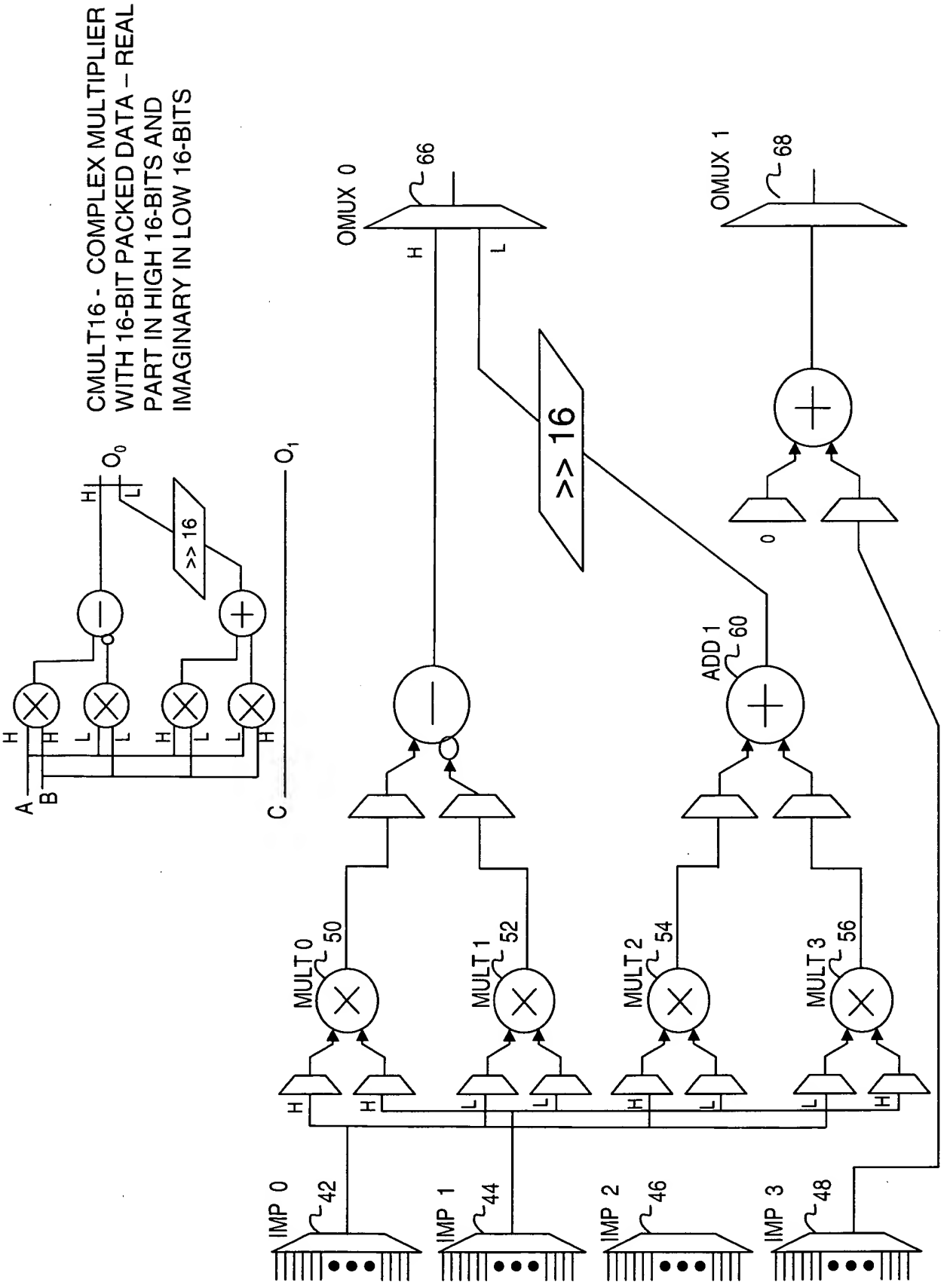
CMULT16 - COMPLEX MULTIPLIER
WITH 16-BIT PACKED DATA – REAL
PART IN HIGH 16-BITS AND
IMAGINARY IN LOW 16-BITS
A
B
C
H
L
O_0
O_1
>> 16
OMUX 0
66
OMUX 1
68
ADD 1
60
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48
0

FIG. 3H

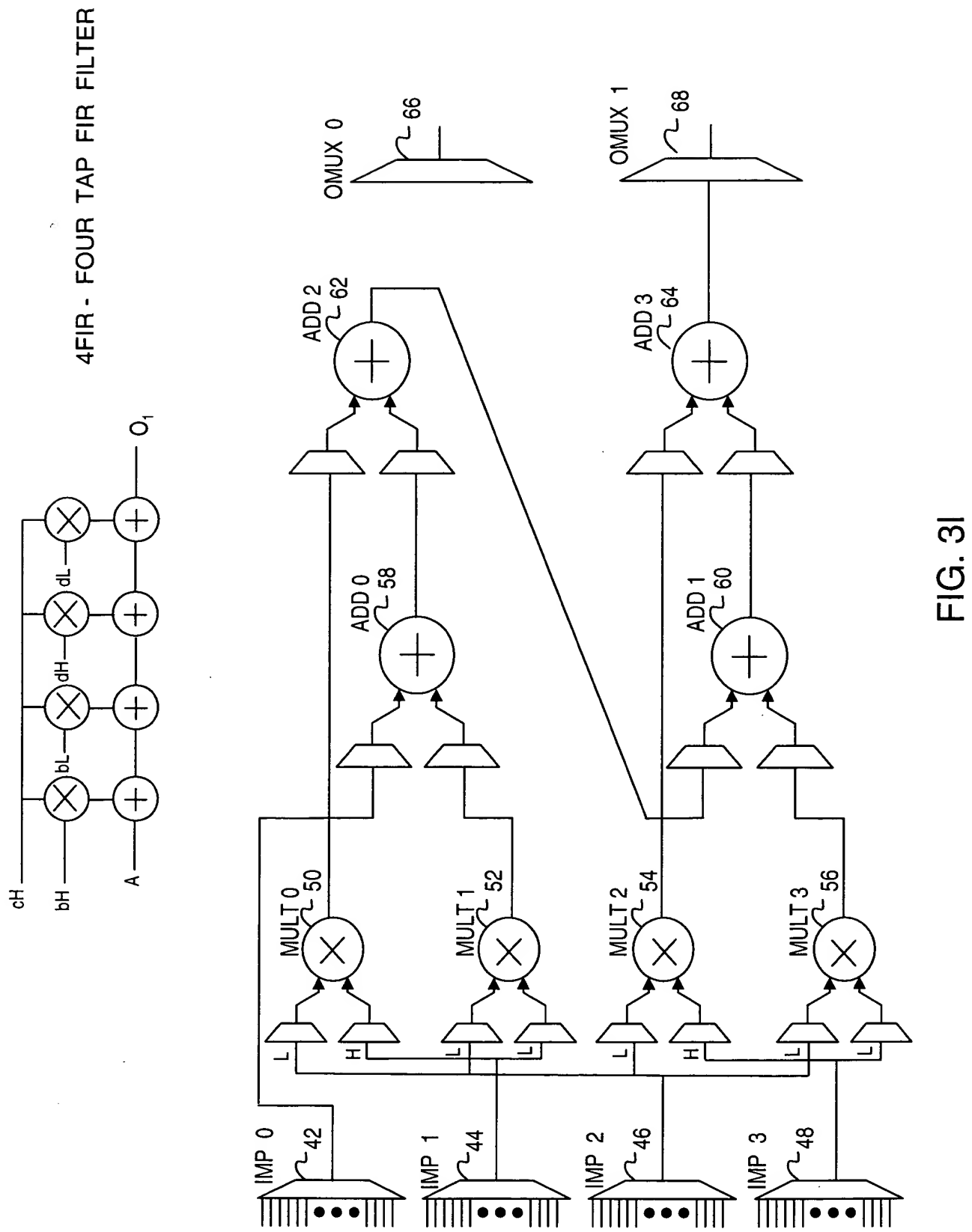
4FIR - FOUR TAP FIR FILTER
cH
bH
bL
dH
dL
A
O_1
OMUX 0
66
OMUX 1
68
ADD 2
62
ADD 3
64
ADD 0
58
ADD 1
60
MULT 0
50
MULT 1
52
MULT 2
54
MULT 3
56
L
H
IMP 0
42
IMP 1
44
IMP 2
46
IMP 3
48

FIG. 3I

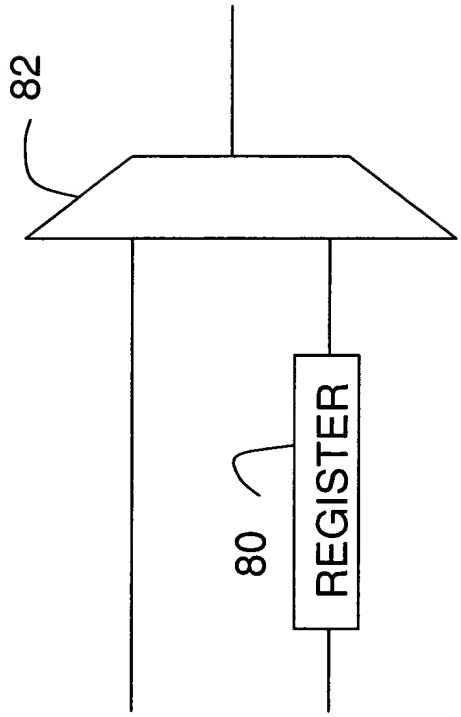
82
80
REGISTER

FIG. 4

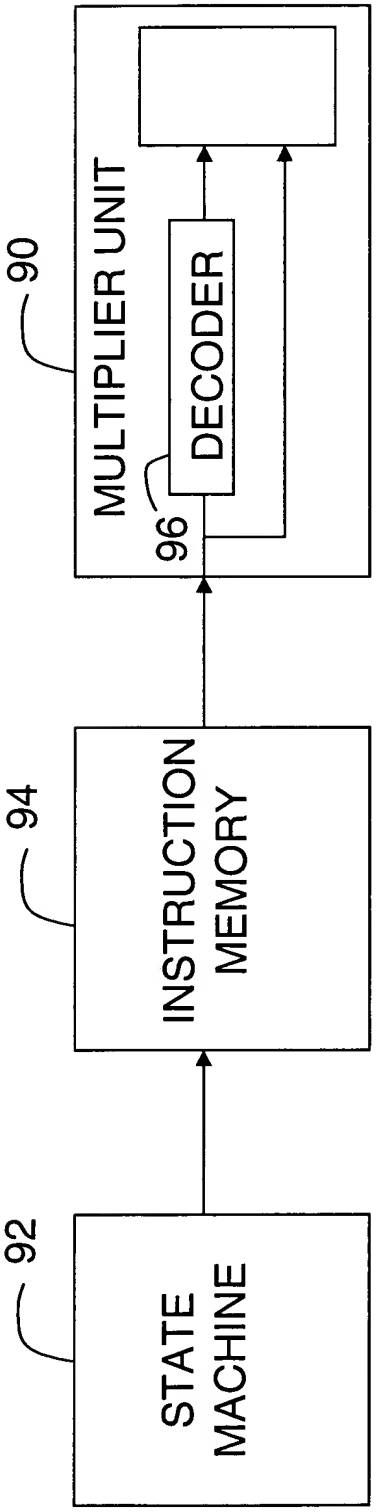
90
MULTIPLIER UNIT
96
DECODER
94
INSTRUCTION MEMORY
92
STATE MACHINE

FIG. 5

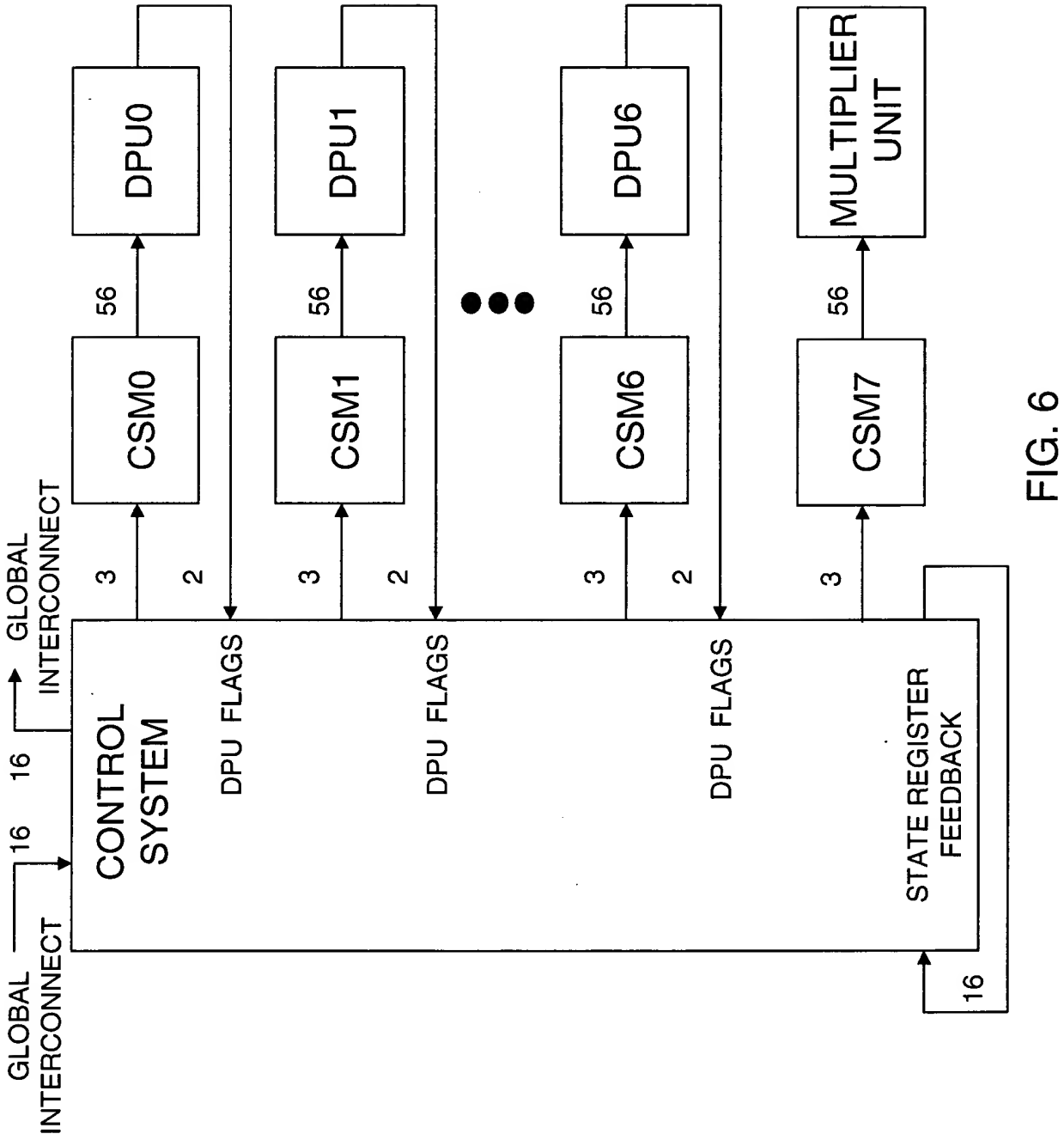
GLOBAL INTERCONNECT
16
16
GLOBAL INTERCONNECT
CONTROL SYSTEM
3
2
DPU FLAGS
CSM0
56
DPU0
CSM1
DPU1
CSM6
DPU6
CSM7
MULTIPLIER UNIT
STATE REGISTER FEEDBACK
16

FIG. 6

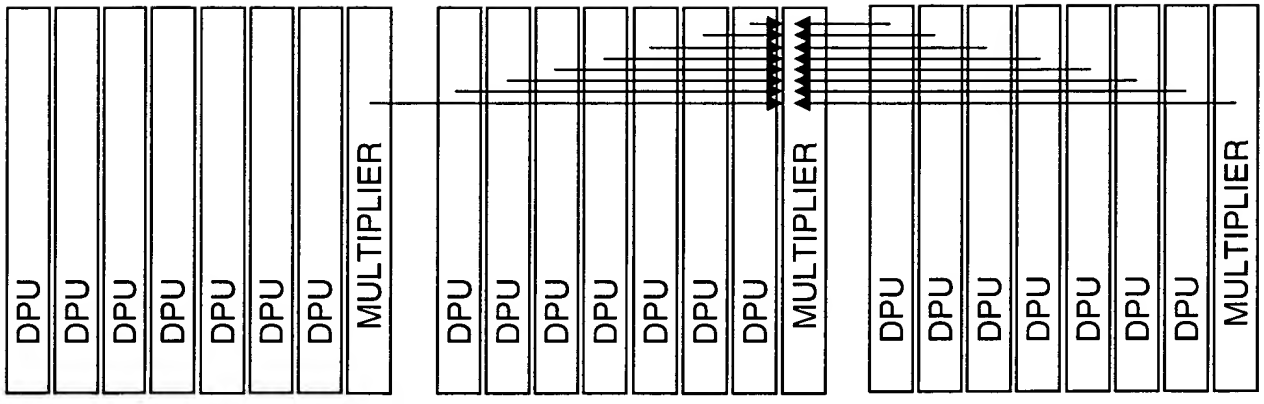
DPU
DPU
DPU
DPU
DPU
DPU
DPU
MULTIPLIER
DPU
DPU
DPU
DPU
DPU
DPU
DPU
MULTIPLIER
DPU
DPU
DPU
DPU
DPU
DPU
DPU
MULTIPLIER

FIG. 7

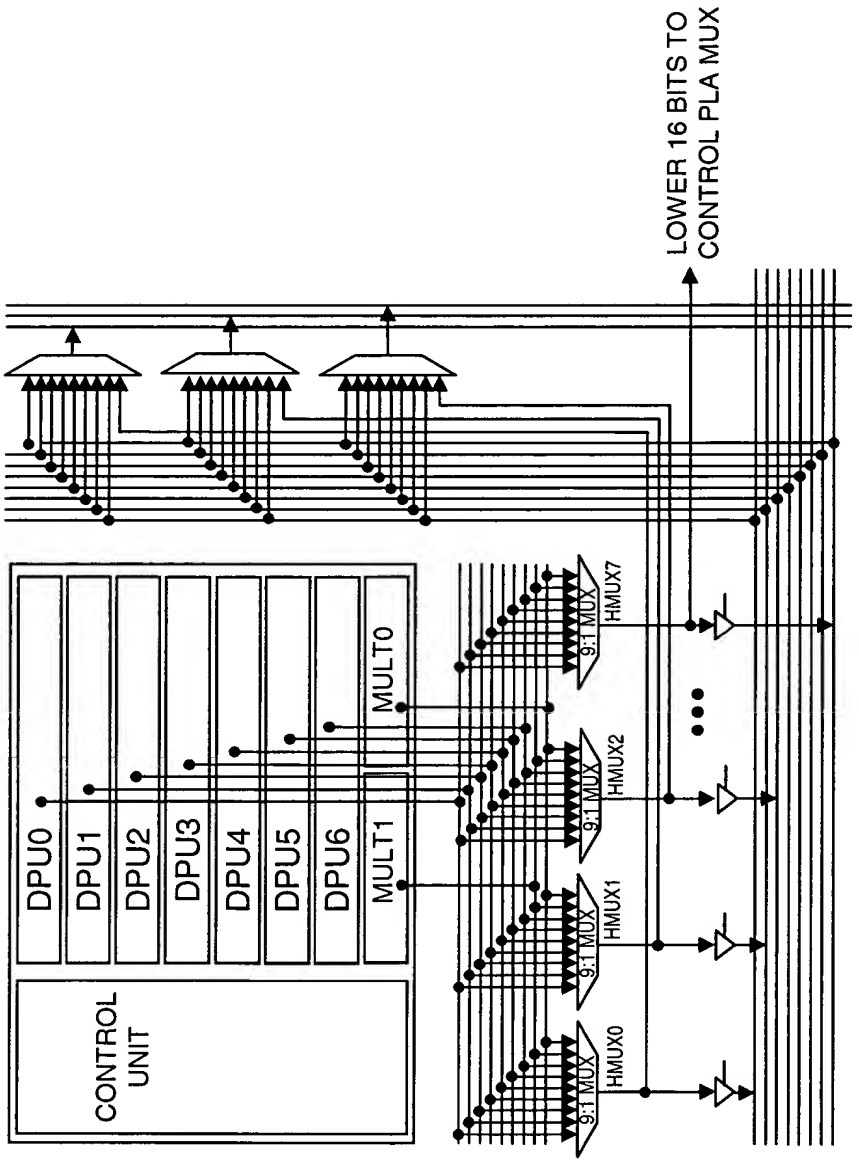
LOWER 16 BITS TO
CONTROL PLA MUX
DPU0
DPU1
DPU2
DPU3
DPU4
DPU5
DPU6
MULT0
MULT1
CONTROL
UNIT
9:1 MUX
HMUX7
9:1 MUX
HMUX2
9:1 MUX
HMUX1
9:1 MUX
HMUX0

FIG. 8

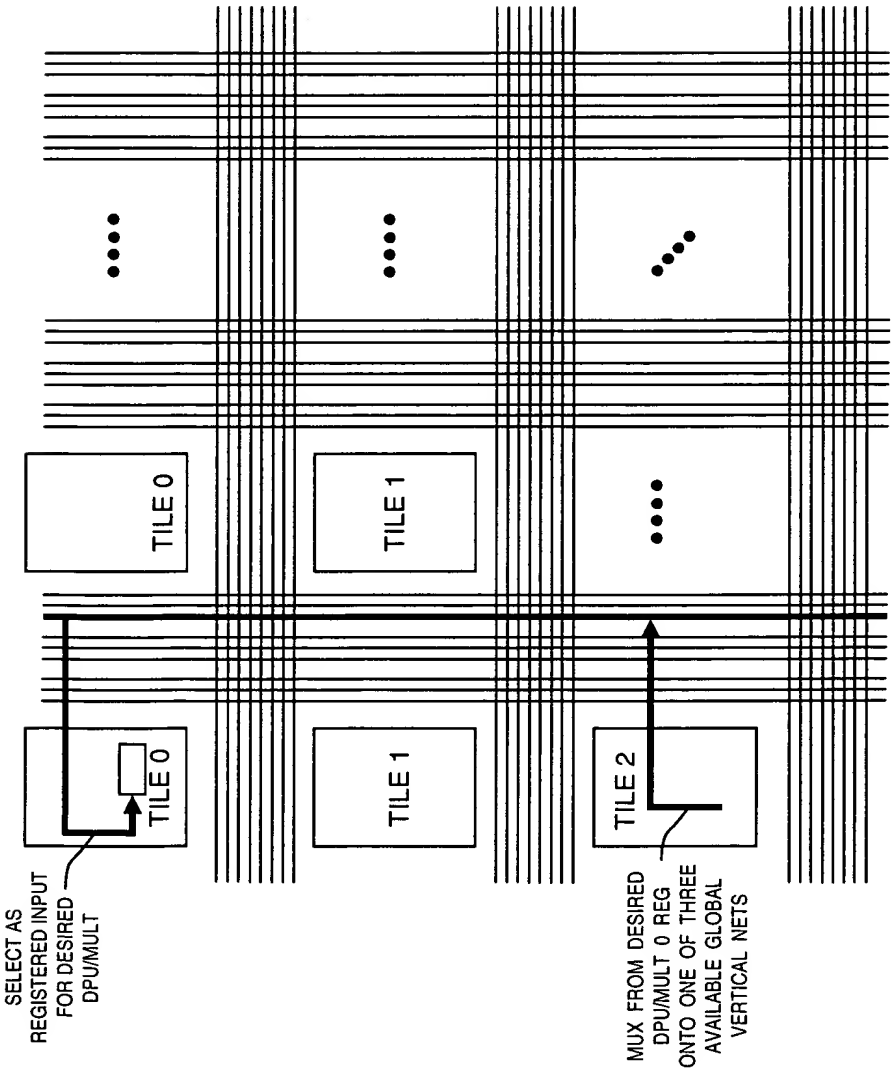
TILE 0
TILE 1
TILE 0
TILE 1
TILE 2
SELECT AS REGISTERED INPUT FOR DESIRED DPU/MULT
MUX FROM DESIRED DPU/MULT 0 REG ONTO ONE OF THREE AVAILABLE GLOBAL VERTICAL NETS

FIG. 9

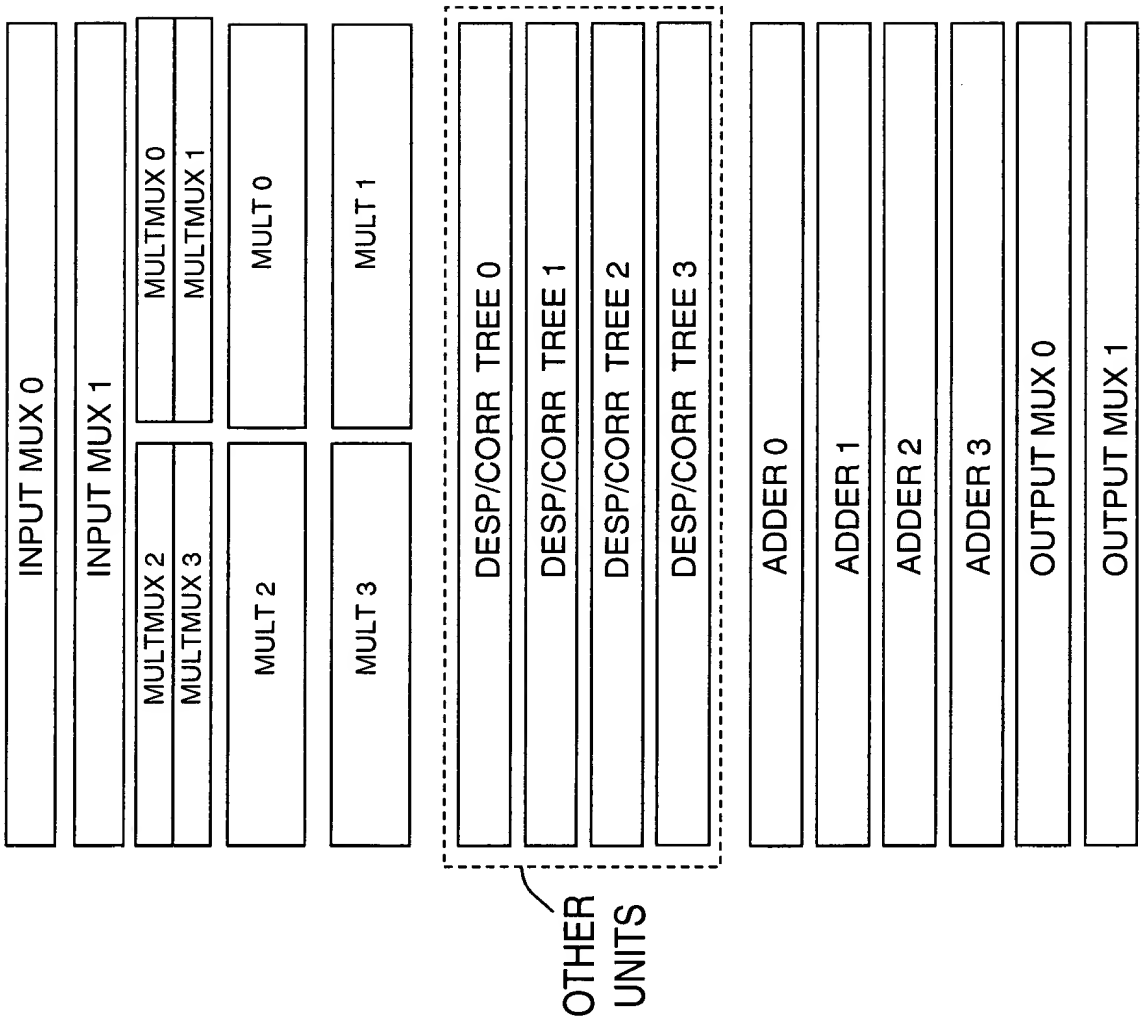
INPUT MUX 0
INPUT MUX 1
MULTMUX 2
MULTMUX 3
MULTMUX 0
MULTMUX 1
MULT 2
MULT 3
MULT 0
MULT 1
DESP/CORR TREE 0
DESP/CORR TREE 1
DESP/CORR TREE 2
DESP/CORR TREE 3
OTHER UNITS
ADDER 0
ADDER 1
ADDER 2
ADDER 3
OUTPUT MUX 0
OUTPUT MUX 1

FIG. 10

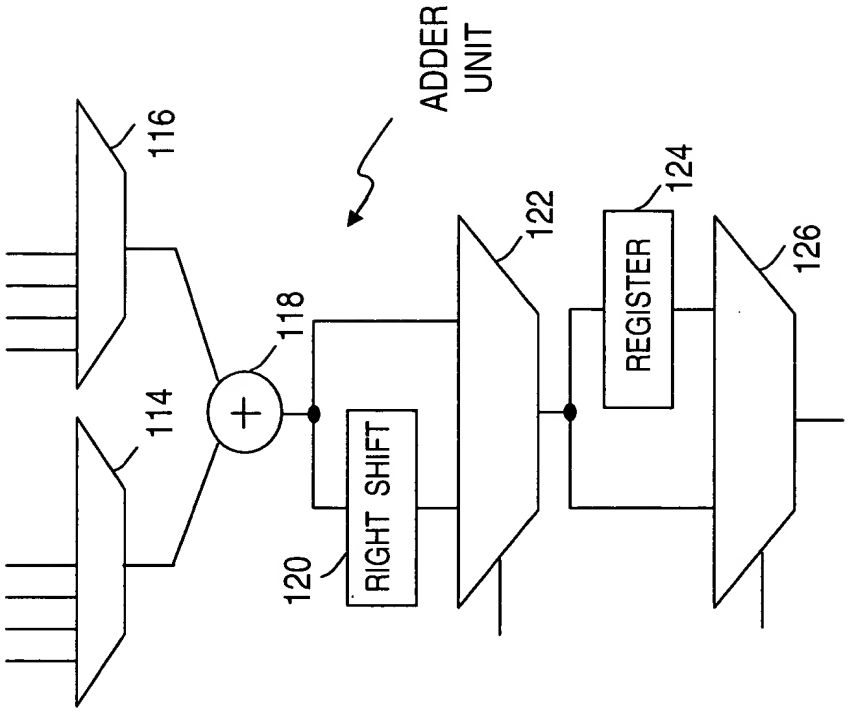
ADDER UNIT
116
114
118
120
RIGHT SHIFT
122
REGISTER
124
126

FIG. 12

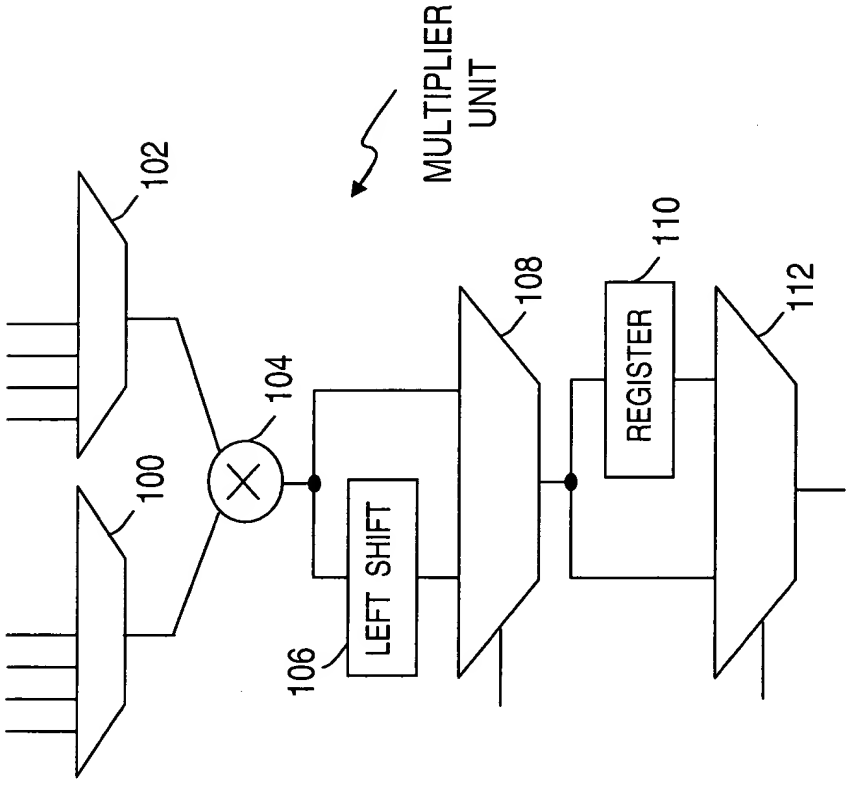
MULTIPLIER UNIT
102
100
104
106
LEFT SHIFT
108
REGISTER
110
112

FIG. 11

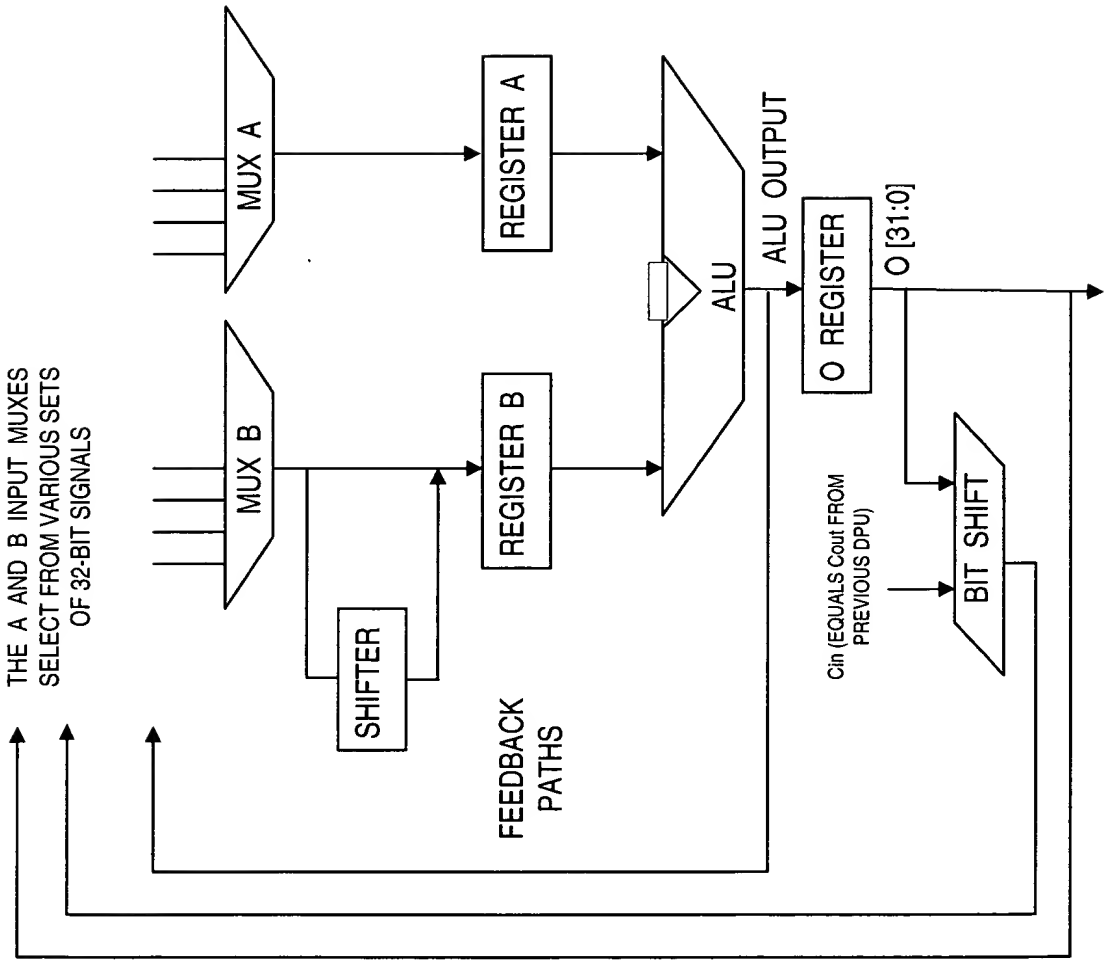
THE A AND B INPUT MUXES
SELECT FROM VARIOUS SETS
OF 32-BIT SIGNALS
MUX A
MUX B
SHIFTER
REGISTER A
REGISTER B
FEEDBACK
PATHS
ALU
ALU OUTPUT
O REGISTER
O [31:0]
Cin (EQUALS Cout FROM
PREVIOUS DPU)
BIT SHIFT
DPU OUTPUT

FIG. 13